RL78/G13

Timer Array Unit (Interval Timer)

R01AN0456EJ0100
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Introduction

This application note describes the interval timer function of the timer array unit (TAU). This unit inverts the LED indication each time a timer interrupt occurs. Also, it changes the timer interrupt cycle time based on the number of times the switch is pressed.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

This application note shows example settings for using timer interrupts (INTTM00) from the interval timer and interrupts (INTP0) generated on pin input edge detection. The TAU inverts the LED indication each time a timer interrupt (INTTM00) occurs. Also, this unit changes the timer interrupt (INTTM00) cycle time based on the number of times the switch (SW) is pressed.

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 shows the timer and its interrupt operation.

Table 1.1 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer array unit (channel 0)	Time interval control for inversion of the P10 pin output (LED indication)
P10	Output port for LED indications
P137/INTP0	Switch input for changing the timer interrupt (INTTM00) cycle time

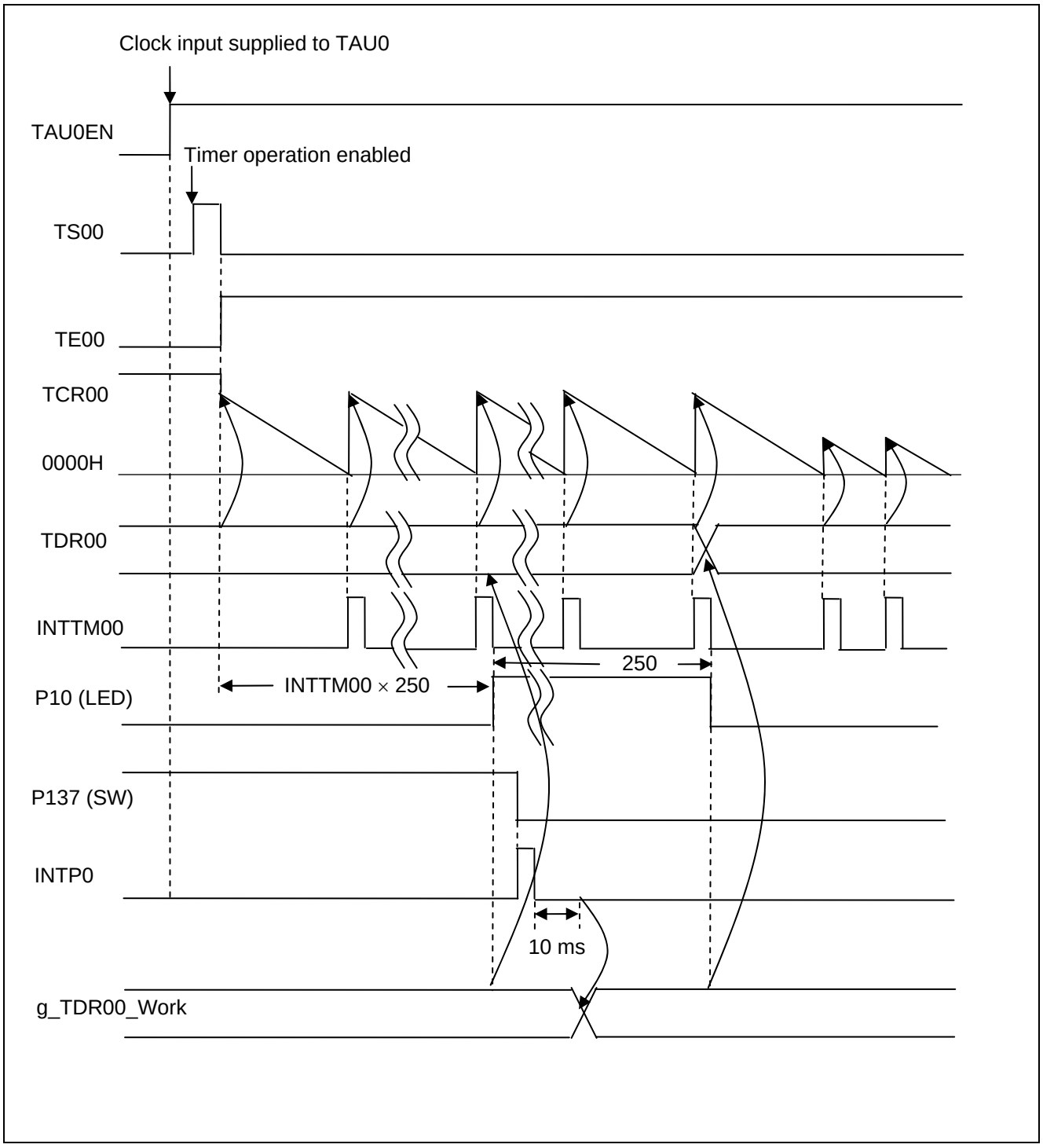

Figure 1.1 Overview of Timer Operation and Interrupts

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVI}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment	CubeSuite + V1.00.01 from Renesas Electronics Corp.
C compiler	CA78K0R V1.20 from Renesas Electronics Corp.

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G13 Initialization (R01AN0451EJ0100) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

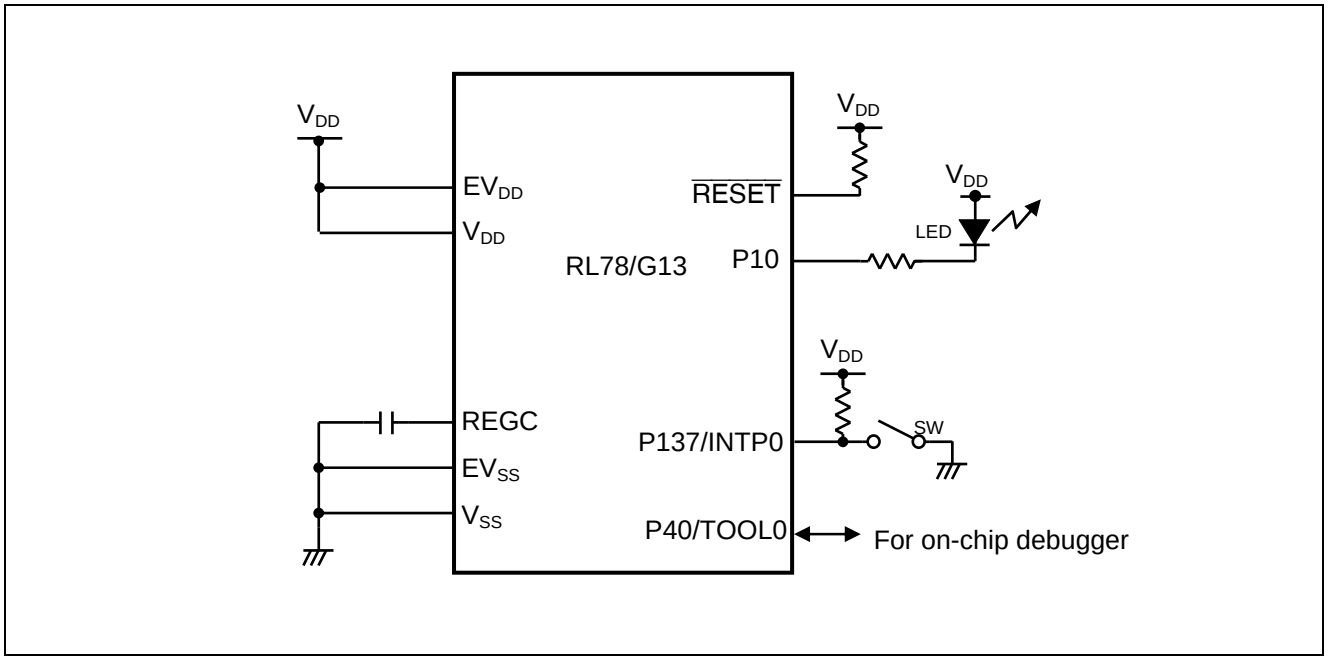

Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P10	Output	Output port for LED indications
P137/INTP0	Input	Switch (SW) input pin (external interrupt request input pin)

5. Description of the Software

5.1 Operation Outline

This application note describes how to set up the interval timer function of TAU0.

This setup is followed by operation for counting the number of timer interrupts (INTTM00) generated by the interval timer. Each time the count reaches 250, the LED indication is inverted. The timer interrupt (INTTM00) cycle time is changed according to the number of times the switch is pressed. The LED on/off cycle time is changed as follows.

500 ms → 250 ms → 125 ms → 62.5 ms → 500 ms → …

(1) Initialize the TAU.
- Use the interval timer mode as the timer operation mode.
- Initialize timer data register 00 (TDR00) to 2 ms.
- Set the timer output enable register to disable operation.
- Use timer interrupts (INTTM00) from timer channel 0.

(2) Initialize the external edge detection interrupt.
- Select a falling edge as the valid edge for INTP0.
- Use INTP0 interrupts.

(3) Execute a HALT instruction to wait for timer interrupts (INTTM00).

(4) After the HALT mode is cancelled by a timer interrupt (INTTM00), the number of INTTM00 interrupts generated is counted.

(5) When the timer interrupt count reaches 250, the LED indication is inverted. The value (g_TDR00_Work) in RAM for the timer data register is set in the timer data register (TDR00).

(6) INTP0 interrupt processing changes the switch input count (INTP0 interrupt count) and g_TDR00_Work value.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
_01_INTP0_EDGE_FALLING_SEL	01h	Selects a falling edge as the valid edge of INTP0.
g_DTR000_Data[]	(64000-1) (32000-1) (16000-1) (8000-1)}	TDR00 settings by number of times the switch is pressed
g_10msCount[]	(5+1) (10+1) (20+1) (40+1)	10 ms timer count values by number of times the switch is pressed

5.4 List of Variables

Table 5.3 lists the global variable that is used by this sample program.

Table 5.3 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
sreg uint8_t	g_SW_Counter	Switch press count	R_INTC0_Interrupt() main() R_InvertLED()
sreg uint16_t	g_TDR00_Work	Value which is set in TDR00 each time the timer interrupt count reaches 250.	R_INTC0_Interrupt() main() R_InvertLED()

5.5 List of Functions

Table 5.4 lists the functions that are used by this sample program.

Table 5.4 Functions

Function Name	Outline
R_TAU0_Channel0_Start	Starts operation of TAU0 channel 0.
R_TAU0_Channel0_Interrupt()	Processes timer interrupts on TAU0 channel 0.
R_InvertLED()	Counts the number of INTTM00 interrupts generated. Inverts the LED indication each time the interrupt count reaches 250.
R_INTC0_Start	Enables INTP0 interrupts.
R_INTC0_Interrupt	Processes INTP0 interrupts.

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_TAU0_Channel0_Start

Synopsis	TAU0 channel 0 operation start
Header	#include "r_cg_macrodriver.h" #include "r_cg_timer.h" #include "r_cg_userdefine.h"
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_TAU0_Channel0_Interrupt()

Synopsis	TAU0 channel 0 timer interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	__interrupt void R_TAU0_Channel0_Interrupt(void)
Explanation	This function calls the function which will invert the LED indication.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_InvertLED()

Synopsis	LED indication inversion processing
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_intc.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_InvertLED(void)
Explanation	This function counts 250 timer interrupts (INTTM00) and then inverts the LED indication (for port latch inversion). It also changes the TDR00 setting to the value specified with g_TDR00_Work.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Start

Synopsis	INTP0 interrupt enable
Header	r_cg_intc.h
Declaration	void R_INTC0_Start(void)
Explanation	This function clears the interrupt request flag. It enables INTP0 interrupts and starts taking in the switch input.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Interrupt()

Synopsis	INTP0 interrupt processing
Header	r_cg_macrodriver.h r_cg_intc.h r_cg_userdefine.h
Declaration	__interrupt void R_INTC0_Interrupt(void)
Explanation	This function processes INTP0 interrupts as they occur. It waits 10 ms and then scans P13.7 (SW input pin). When the switch is pressed, this function changes the g_TDR00_Work value.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

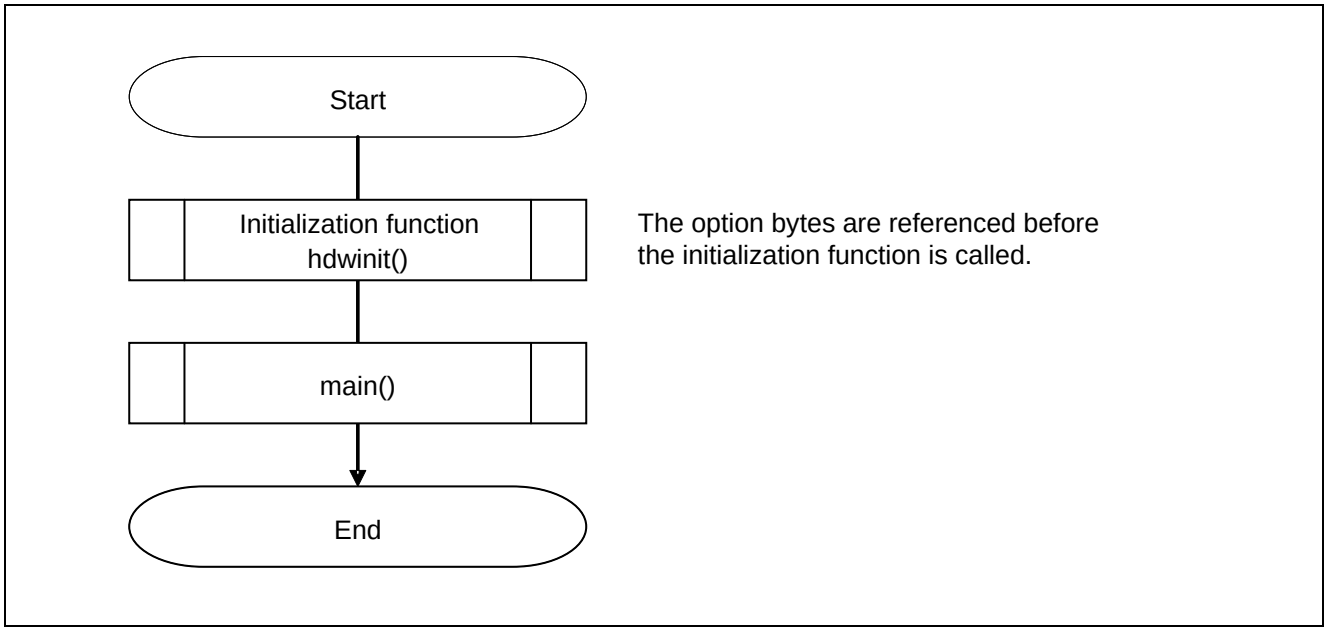

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

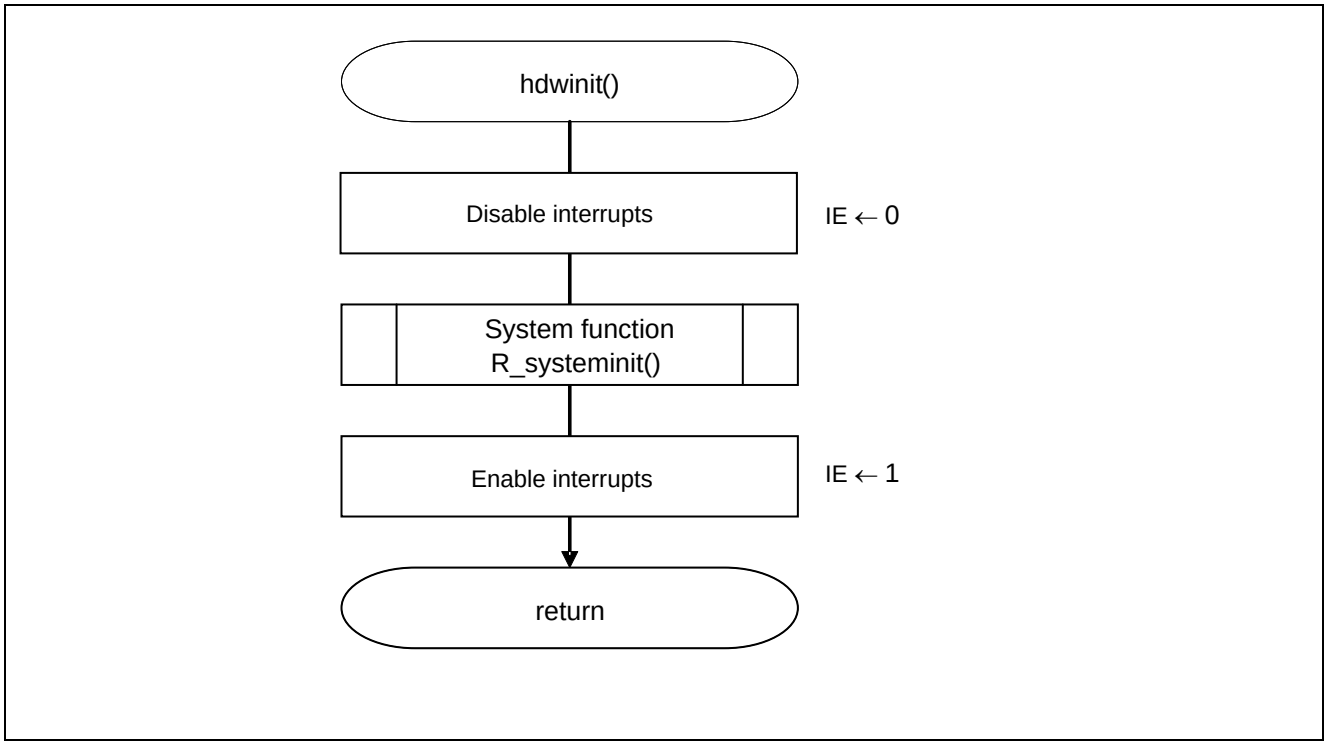

Figure 5.2 Initialization Function

5.7.2 System Function

Table 5.3 shows the flowchart for the system function.

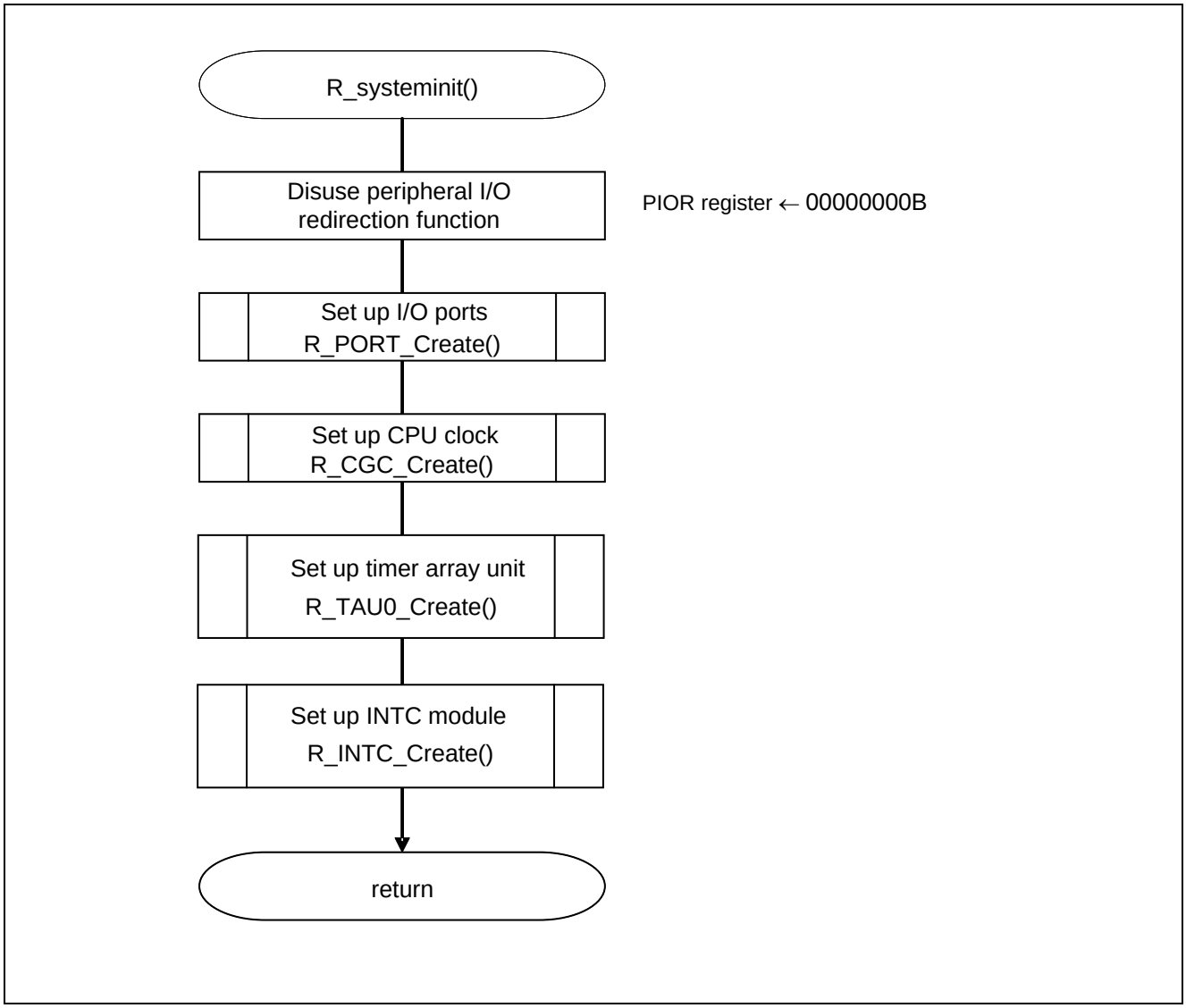

Figure 5.3 System Function

5.7.3 I/O Port Setup

Table 5.4 shows the flowchart for I/O port setup.

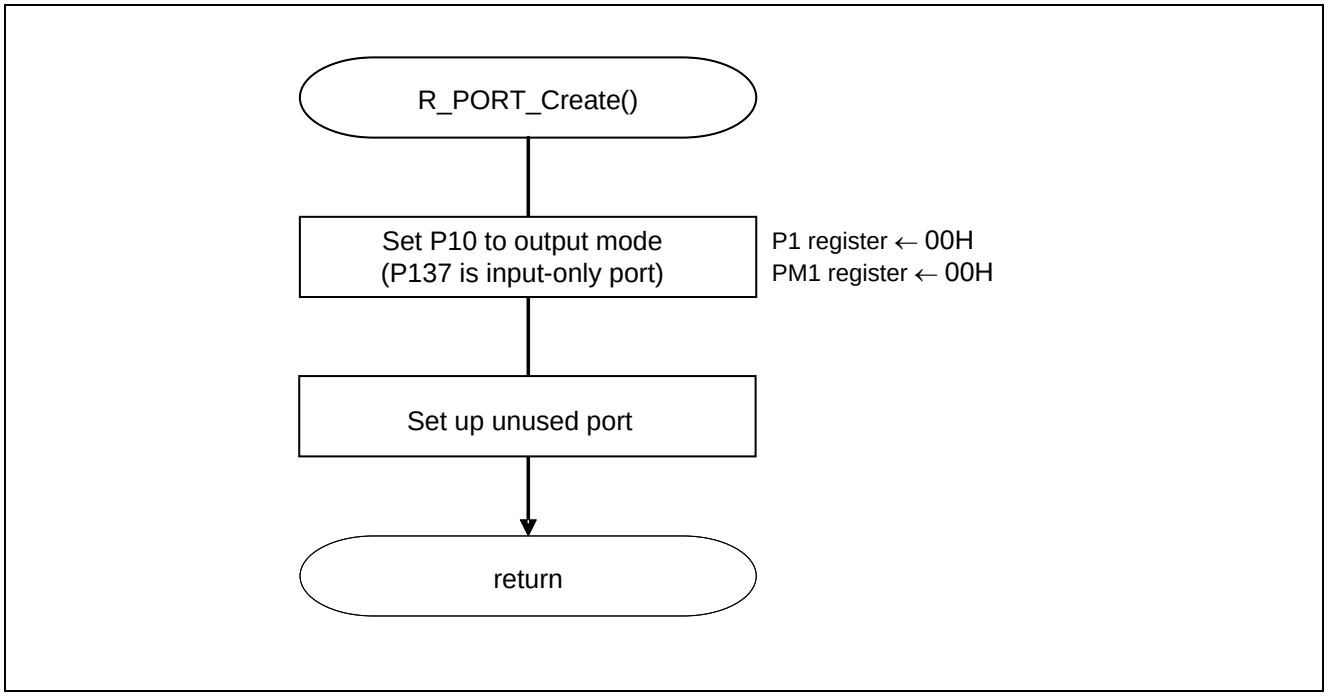

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to VDD or VSS via a separate resistor.

Setting up the LED port

- Port mode register 1 (PM1)
  Select I/O mode for the port.

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
0	0	0	0	0	0	0	**0**

Bit 0

PM10	P10 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

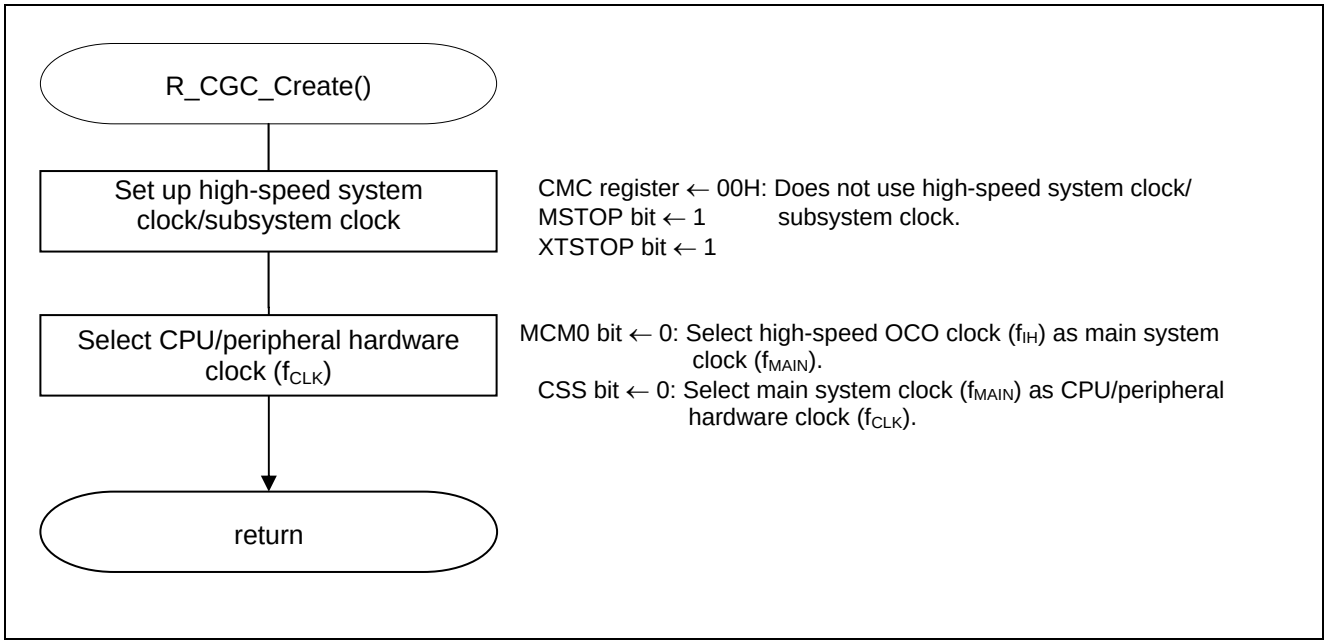
R_CGC_Create()
Set up high-speed system clock/subsystem clock
CMC register ← 00H: Does not use high-speed system clock/ subsystem clock.
MSTOP bit ← 1
XTSTOP bit ← 1
Select CPU/peripheral hardware clock (fCLK)
MCM0 bit ← 0: Select high-speed OCO clock (fIH) as main system clock (fMAIN).
CSS bit ← 0: Select main system clock (fMAIN) as CPU/peripheral hardware clock (fCLK).
return

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100).

5.7.5 Timer Array Unit Setup

Figure 5.6 shows the flowchart for setting up the timer array unit.

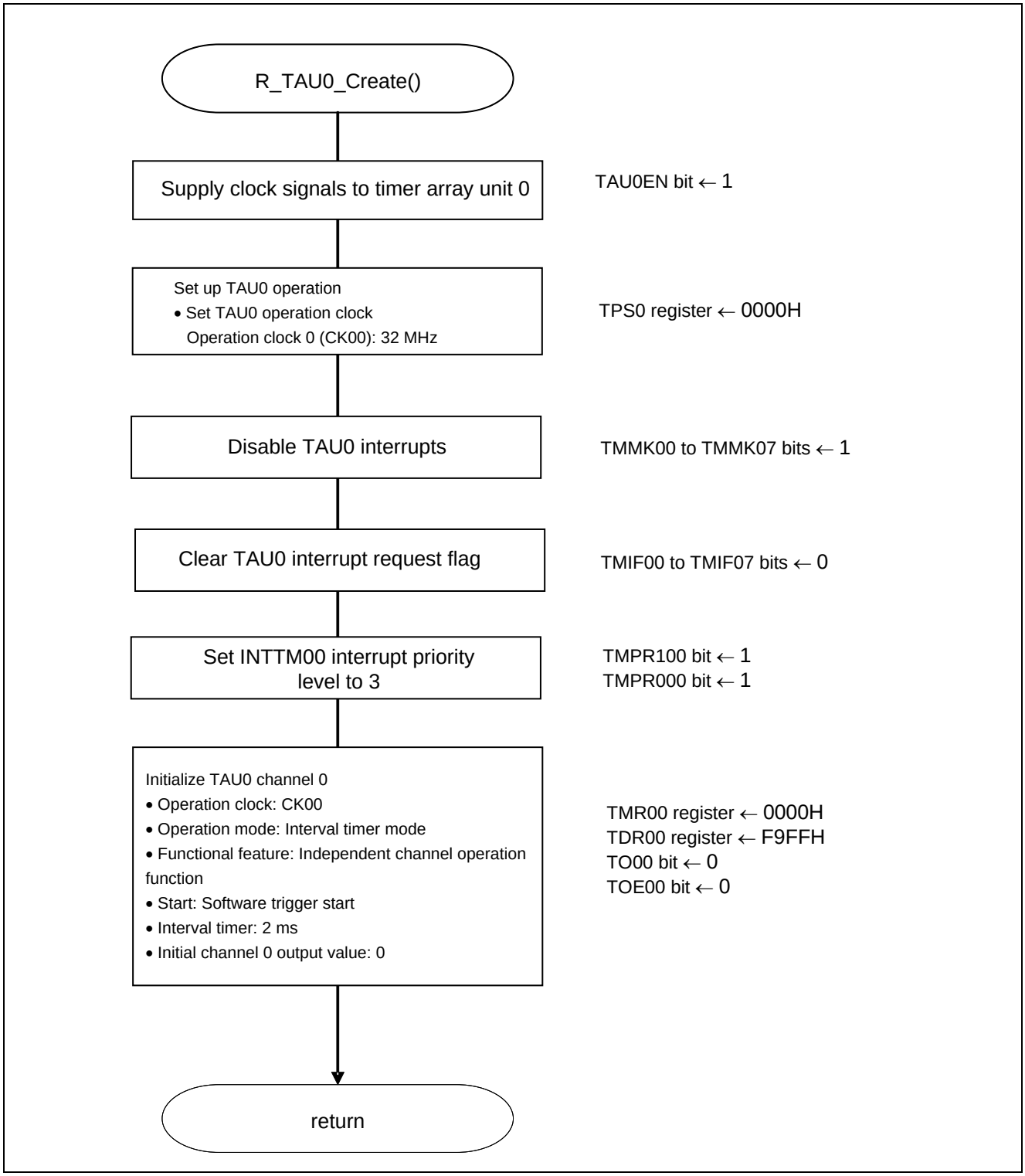
R_TAU0_Create()
Supply clock signals to timer array unit 0
TAU0EN bit ← 1
Set up TAU0 operation
• Set TAU0 operation clock
Operation clock 0 (CK00): 32 MHz
TPS0 register ← 0000H
Disable TAU0 interrupts
TMMK00 to TMMK07 bits ← 1
Clear TAU0 interrupt request flag
TMIF00 to TMIF07 bits ← 0
Set INTTM00 interrupt priority level to 3
TMPR100 bit ← 1
TMPR000 bit ← 1
Initialize TAU0 channel 0
• Operation clock: CK00
• Operation mode: Interval timer mode
• Functional feature: Independent channel operation function
• Start: Software trigger start
• Interval timer: 2 ms
• Initial channel 0 output value: 0
TMR00 register ← 0000H
TDR00 register ← F9FFH
TO00 bit ← 0
TOE00 bit ← 0
return

Figure 5.6 Timer Array Unit Setup

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
  Start supplying clock signals to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)
  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 5 MHz	f_{CLK}= 10 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**32 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	312.5 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156.2 kHz	312.5 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156.2 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.76 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.76 kHz	15.63 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	976 Hz

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up channel 0 operation mode

- Timer mode register 00 (TMR00)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select the software trigger start.
  Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	MASTER00	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15 and 14

CKS001	CKS000	Channel 0 operation clock (f_{MCK}) selection
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	**Operation clock CK02 set by timer clock select register 0 (TPS0)**
1	0	**Operation clock CK01 set by timer clock select register 0 (TPS0)**
1	1	**Operation clock CK03 set by timer clock select register 0 (TPS0)**

Bit 12

CCS00	Channel 0 count clock (f_{TCLK}) selection
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of input signal input from the TI00 pin

Bit 11

MASTER00	Selection between using channel 0 independently or simultaneously with another channel (as a slave or master)
0	**Operates in independent channel operation function or as slave channel in simultaneous channel operation function.**
1	**Operates as master channel in simultaneous channel operation function.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	MASTER00	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 to 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	MASTER00	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Related function	TCR counting operation
0	**0**	**0**	1/**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD000 bit operation varies depending on the operation mode (see the table below)

Operation mode (selected with MD003 to MD001) (See the table above)	MD000	TCR counting operation
• **Interval timer mode (0, 0, 0)** • **Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Configuring the interval timer cycle time

- Timer data register 00 (TDR00)
  Configure the interval timer compare value.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM00) occurrence = (TDR00 setting + 1) × Count clock cycle time

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	**0**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**The TO00 operation stopped by count operation (timer channel output bit).** **Writing to the TO00 bit is enabled.** **The TO00 pin function as data output, and it outputs the level set to the TO00 bit.** **The output level of the TO00 pin can be manipulated be software.**
1	The TO00 operation enabled by count operation (timer channel output bit). **Writing to the TO00 bit is disabled (writing is ignored).** **The TO00 pin functions as timer output, and the TOE00 bit is set or reset depending on the timer operation.** **The TO00 pin outputs the square-wave or PWM depending on the timer operation.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 INTP0 Initialization

Figure 5.7 shows the flowchart for INTP0 initialization.

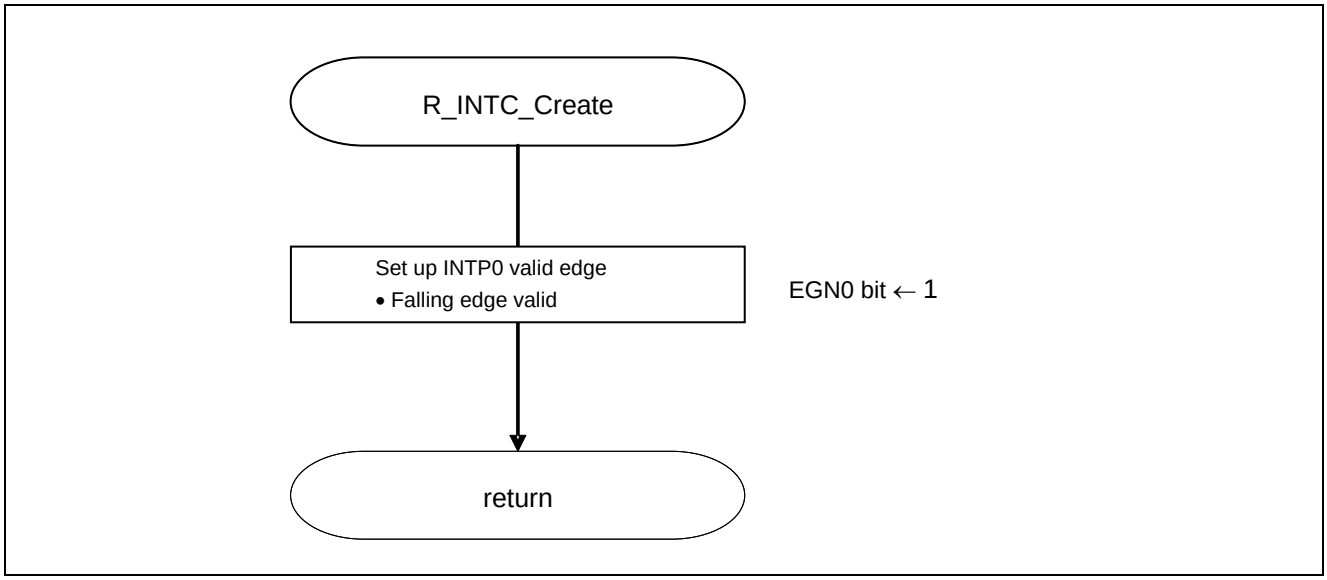

Figure 5.7 INTC Module Setup

Setup for INTP0 pin edge detection

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  Select a valid edge for INTP0

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0
x	x	x	x	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
x	x	x	x	x	x	x	**1**

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled.
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Main Processing

Figure 5.8 shows the flowchart for main processing.

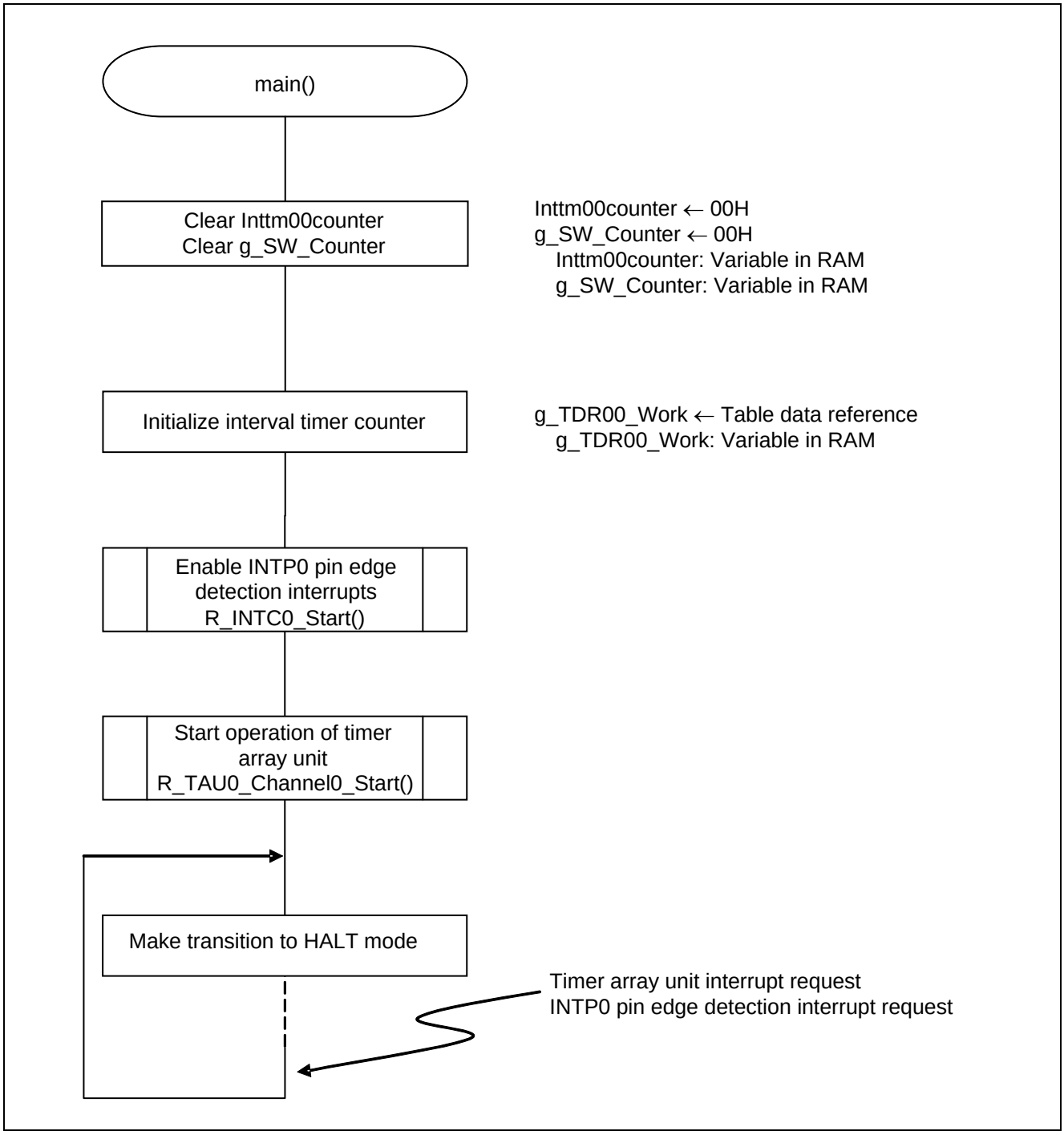

Figure 5.8 Main Processing

5.7.8 INTP0 Operation Start

Figure 5.9 shows the flowchart for starting INTP0 operation.

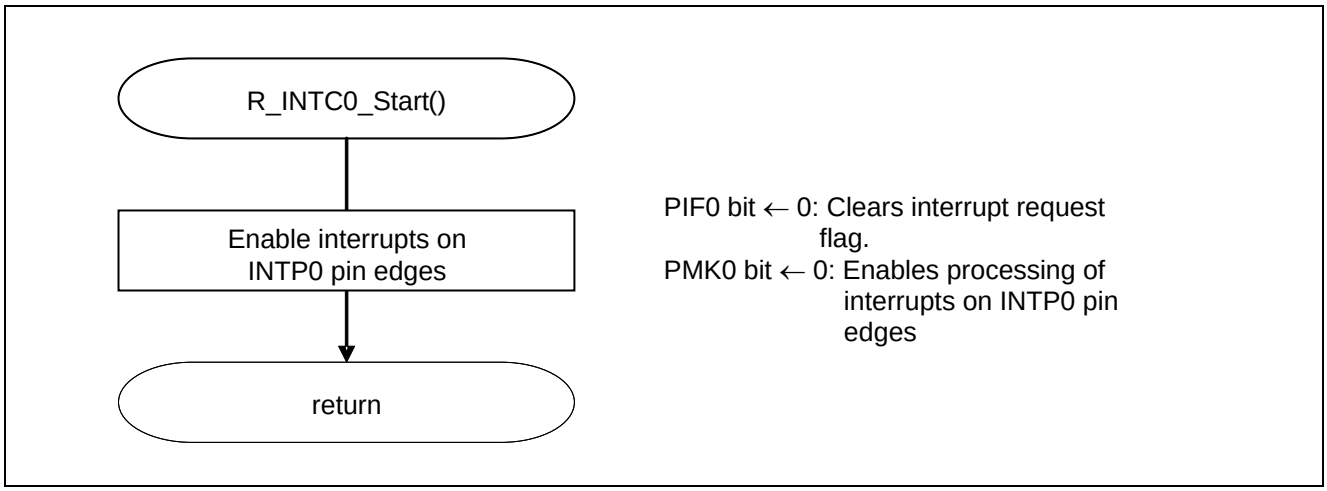
R_INTC0_Start()
Enable interrupts on INTP0 pin edges
return
PIF0 bit ← 0: Clears interrupt request flag.
PMK0 bit ← 0: Enables processing of interrupts on INTP0 pin edges

Figure 5.9 INTP0 Operation Start

Setup for INTP0 Interrupts

- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	**0**	x	x

Bit 2

PIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	**0**	x	x

Bit 2

PMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For detailed information about setting the registers, see RL78/G13 User's Manual: Hardware.

5.7.9 Timer Array Unit 0 Operation Start

Figure 5.10 shows the flowchart for starting timer array unit operation.

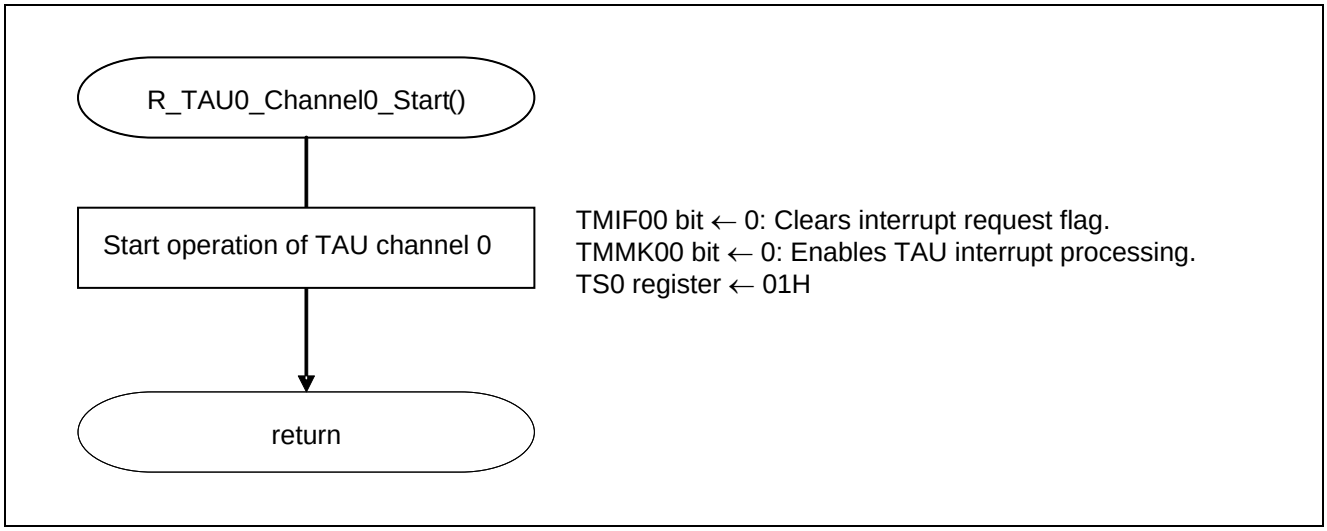
R_TAU0_Channel0_Start()
Start operation of TAU channel 0
return
TMIF00 bit ← 0: Clears interrupt request flag.
TMMK00 bit ← 0: Enables TAU interrupt processing.
TS0 register ← 01H

Figure 5.10 Timer Array Unit 0 Operation Start

Configuring the timer interrupt

- Interrupt request flag register (IF1L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Enable interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.10 INTTM00 Interrupt Processing

Figure 5.11 shows the flowchart for INTTM00 interrupt processing.

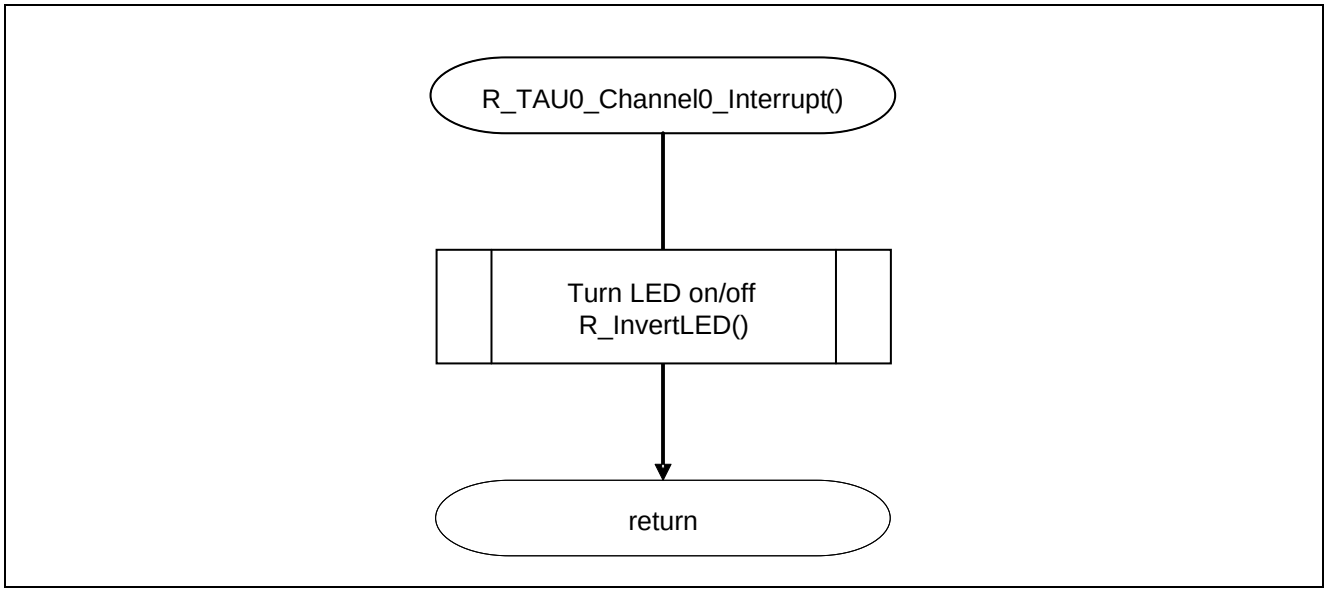

Figure 5.11 INTTM00 Interrupt Processing

5.7.11 LED Turn-On/Off Processing

Figure 5.12 shows the flowchart for LED turn-on/off processing.

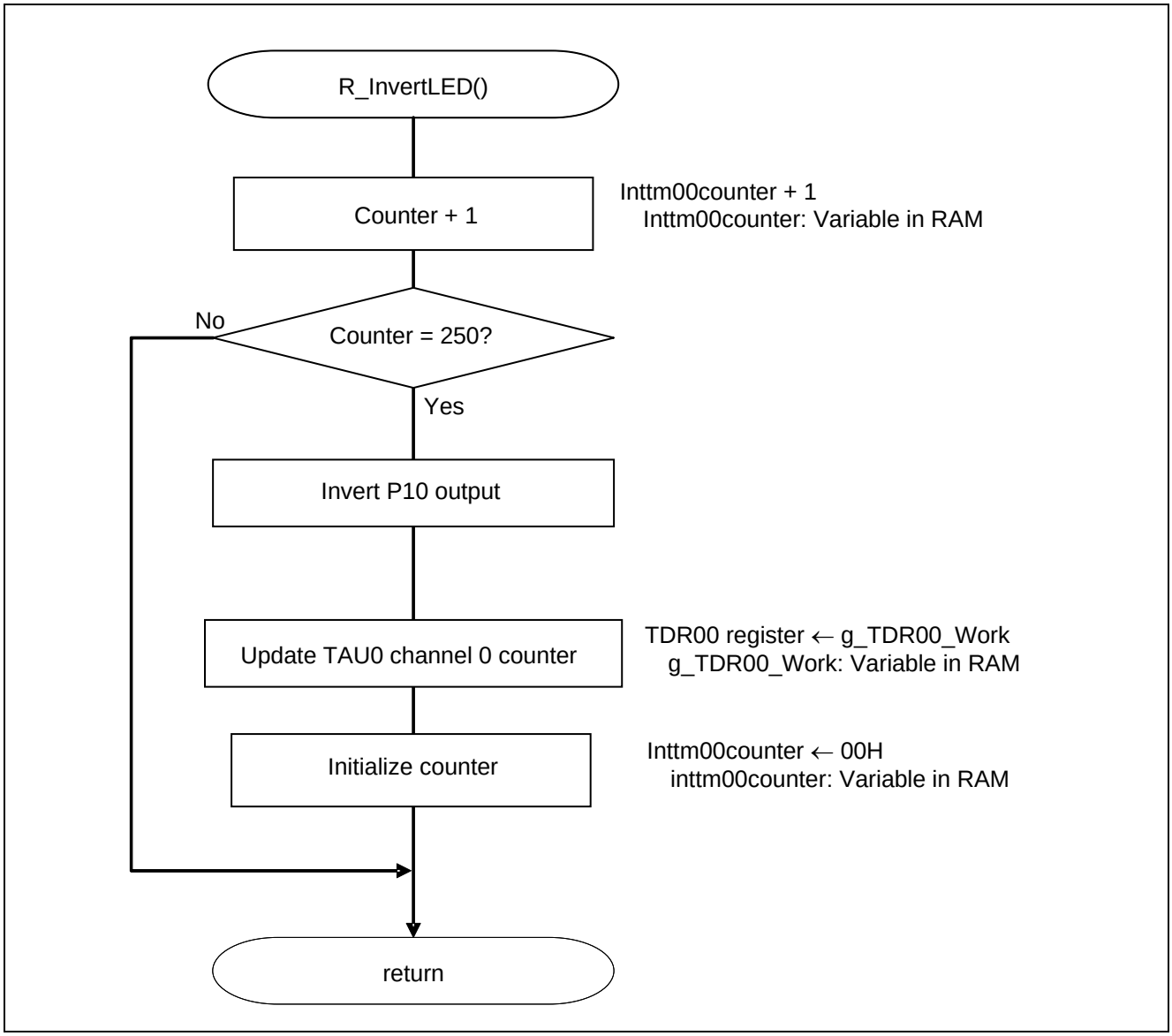

Figure 5.12 Checking Whether 500 ms Have Elapsed

5.7.12 INTP0 Interrupt Processing

Figures 5.13 and 5.14 show the flowchart for INTP0 interrupt processing.

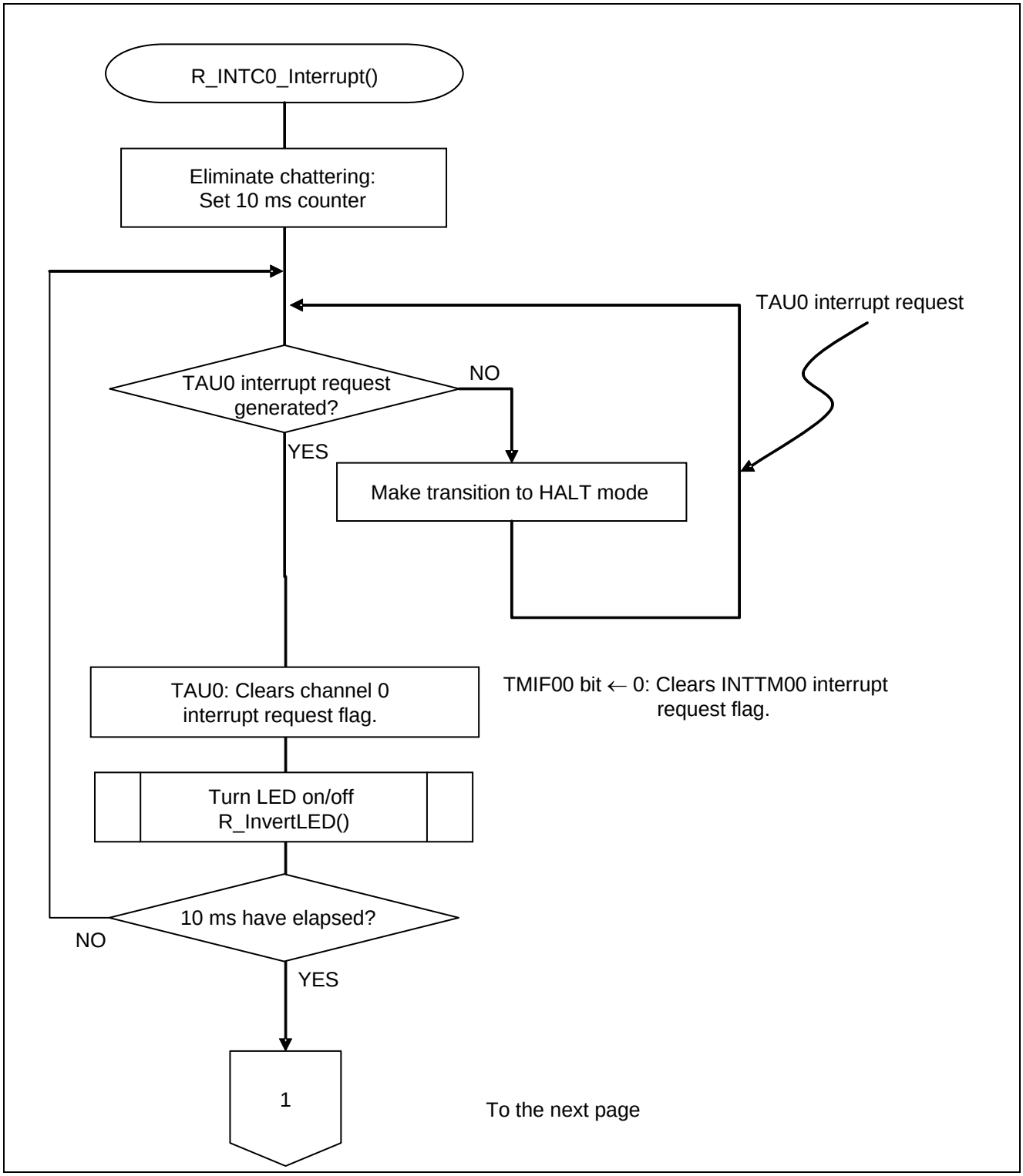

Figure 5.13 INTP0 Interrupt Processing (1/2)

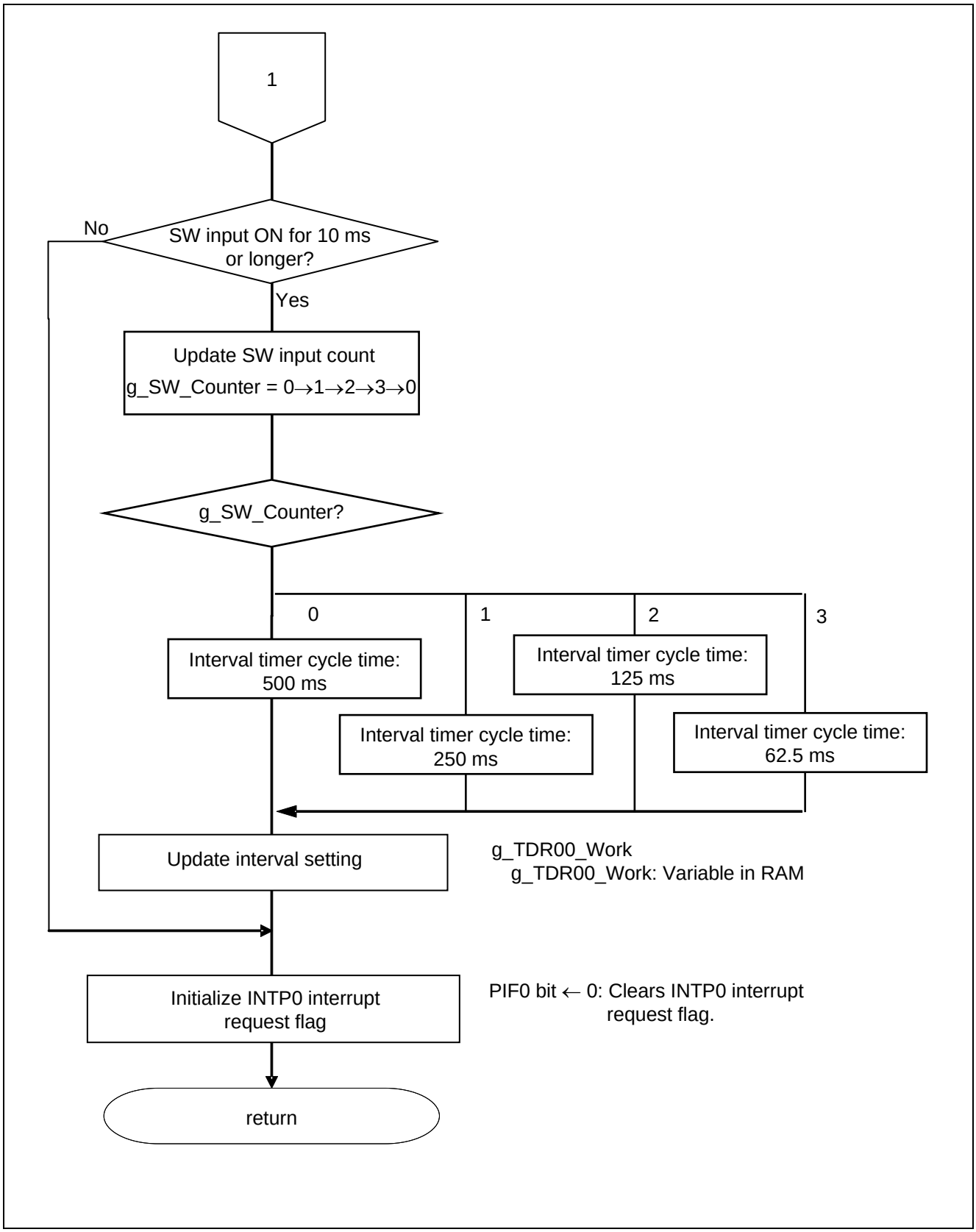

Figure 5.14 INTP0 Interrupt Processing (2/2)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware Rev.0.07 (R01UH0146EJ0007)

RL78 Family User's Manual: Software Rev.1.00 (R01US0015EJ0100)

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G13 Timer Array Unit (Interval Timer)

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2011	—	First edition issued

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1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
  - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
  - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
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Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
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